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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,425	03/30/2004	Eric C. Samson	42P18586	5702

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EXAMINER	
BAE, JI H	

ART UNIT	PAPER NUMBER
2115	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,425	SAMSON, ERIC C.	
	Examiner	Art Unit	
	JI H. BAE	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-9 and 11-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-9 and 11-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2-21-2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 18 February 2008 has been entered.

Response to Arguments

Applicant's arguments filed on 18 February 2008 have been fully considered but they are not persuasive.

Applicant has amended claim 1 to recite a data store for storing the results of a first task performed by a first processor, and that an interrupt is signaled by a second processor to a first processor to indicate that the data store is available for use by the first processor. Independent claims 8, 14, and 21 have been similarly amended.

Deering, which was cited as the primary reference in the previous office action, teaches a first processor [Fig. 4, host CPU 102] and a second processor [graphics system 112]. The host CPU generates data and commands for the graphics system, which may be stored in the main memory 106, or other memories. The graphics system is able to retrieve the commands and data from the various memories for processing [col. 8, lines 32-53].

Luu, which was cited as a secondary reference in the previous office action, teaches a graphics processing system wherein a CPU issues a set of graphics commands to a GPU. The CPU enters a power saving mode after commands have been issued. When the GPU has

completed processing of the graphics commands, it issues an interrupt to the CPU to indicate that it is ready for additional commands [col. 4, lines 39-49].

Thus, Deering teaches a "data store" [main memory 106] for storing commands issued from a "first processor" [host CPU 102] for a "second processor" [graphics system 112]. Luu teaches that once a GPU has completed processing of the commands that have been issued, it signals an interrupt to a CPU to indicate that additional commands may be issued. In a system representing the combined teachings of Deering with Luu, once an interrupt has been issued from the graphics system to the host CPU to indicate that additional commands may be issued (as taught by Luu), the host CPU will then generate additional graphics data and commands and store them in the main memory or other appropriate memory (as taught by Deering). Therefore, the interrupt taught by Luu indicates that ***the main memory is ready for additional commands from the host CPU.*** As such, the examiner submits that the applicant's amendments do not further define over the cited prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deering, U.S. Patent No. 6,313,838 B1, in view of Lin et al., U.S. Patent Application Publication No. 2003/0233592 A1, in view of Luu et al., U.S. Patent no. 7,256,788 B1.

Regarding claim 1, Deering teaches:

providing a first processor of the system with a first task to perform [host CPU, Fig. 4];

providing a second processor of the system with a second task to perform, wherein performance of the second task will use a result of the first task [graphics accelerator/system, Fig. 4].

Deering does not teach requesting an adjustment to an operating point of one of the first and second processors.

Lin teaches:

requesting an adjustment to an operating point of a graphics processor to better manage power consumption in the electronic system, based on the time between completion of a task and its deadline [paragraph 12, 14, 29, and 30].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Lin with Deering by implementing the clock scaling techniques of Lin in the system of Deering. Both Lin and Deering are directed towards graphics processors with real-time demands – specifically, rendering image frames at a desired frame rate. The teachings of Lin would improve the system of Deering by allowing Deering to operate at a desired frame rate, while at the same time preventing the unnecessary consumption of power [paragraphs 9-11].

Although the combination of Lin/Deering teaches the aforementioned subject matter, neither Lin nor Dearing teaches the step of **signaling an interrupt to the first processor by the second processor upon completion of a second task** [claim 1 amendments].

Luu teaches a graphics processing system wherein a CPU issues a set of graphics commands to a GPU. After issuing the commands, the CPU transitions to a power saving mode while the graphics processing is carried out by the GPU. When the graphics processing is completed, the GPU sends an interrupt to the CPU to indicate that it is ready to receive additional commands [col. 4, lines 39-49].

It would have been obvious to one of ordinary skill in the art to modify the combination of Lin/Deering by implementing the CPU power saving and interrupt steps taught by Luu. Lin/Deering and Luu are both directed towards power saving techniques for graphics processing systems. Lin/Deering teaches a similar configuration to Luu; specifically, both Lin/Deering and Luu teach a processor which issues commands for rendering images to a graphics processor [Lin Fig. 3, Deering Fig. 4, Luu Fig. 2]. Luu teaches that in such systems, power savings may be achieved by putting the CPU (which is simply waiting for acknowledgement from the graphics processor that it is ready for additional commands) into a power saving mode. Therefore, the teachings of Luu would improve upon the combination of Lin/Deering by putting the CPU to sleep while the GPU renders the image, thus providing an additional measure of power savings.

The combination of Deering/Lin/Luu also teaches a data store for storing the result of a first task from the first processor, and that the interrupt issued by the second processor signals that additional commands may be sent to the second processor by storing them in the main memory [see "Response to Arguments].

Regarding claims 2 and 3, Lin teaches decreasing or increasing the clock frequency, depending on if the deadline was met [paragraph 30].

Regarding claim 4, Lin and Deering teach that the tasks related to describing and rendering images at a desired frame rate.

Regarding claim 5, Lin teaches measuring the amount of time needed for the graphics processor to render a frame. Additionally, it would have been obvious to one of ordinary skill in the art to measure any other time period that would contribute to the graphics processor meeting its targeted frame rate.

Regarding claim 8, Lin teaches a method comprising:

providing a processor with a workload that has a real-time demand [desired frame rate, paragraph 24 and 25]; and

setting a processor clock frequency requirement for the processor based on a deadline margin for the real-time demand [paragraphs 29 and 30, Fig. 4 and 6].

Deering teaches measuring the rendering time by measuring, for each polygon in the frame, a time between identifying each polygon to be rendered and a start time for the rendering [identifying, col. 3, lines 61-67, rendering set-up time, col. 4, lines 30-32].

Luu teaches that the GPU sends an interrupt to the CPU when it has completed rendering in order to indicate that it is ready to receive additional commands [col. 4, lines 39-49].

Regarding claim 9, Lin teaches the that real-time demand is a target frame rate.

Regarding claims 12 and 13, Lin teaches that the margin comprises a measurement of the time between completion of rendering an image and a start of display, and an estimate of the time needed to render and the target frame rate [paragraph 10, 30].

Regarding claims 14-24, the combination of Lin/Deering/Luu teaches the method of claims 1-13. Lin/Deering/Luu also teach the system and article of manufacture to implement the claimed method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JI H. BAE whose telephone number is (571)272-7181. The examiner can normally be reached on Monday-Friday, 10 am to 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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